Rao, G. Nagesh

From: Bob Crawford [crawford@ip-firm.com]
Sent: Wednesday, July 28, 2010 3:26 PM
To: Rao, G. Nagesh
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Subject: Serial No. 10/539,549 (BE02004US1/NXPS.420PA) - proposed claims amendments
Attachments: Examiner Proposal NXPS.420PA -28JULY2010.doc

Dear Examiner Rao,

Please see attached which we understand should comport with your proposed claim amendments to render the case allowable. Please appreciate that should such amendments be implemented, agreement to the amendments would be without prejudice to further prosecution of the unamended claims in a related (e.g., continuation) application.

Best regards,
Bob

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Reply under 37 C.F.R. 1.116
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	MAGNEE, et al.	Examiner:	Rao, G.
Serial No.:	10/539,549	Group Art Unit:	1714
Filed:	June 16, 2005	Docket No.:	BE020044US1 (NXPS.420PA)
Title:	METHOD OF MANUFACTURING A SEMICONDUCTOR DEVICE		

In the Claims:

1. (Currently amended) A method of manufacturing a semiconductor device on a region of silicon oxide situated next to a region of monocrystalline silicon at a surface of a semiconductor body, the method comprising the steps of:

1) forming a layer of arsenic on the region of monocrystalline silicon by heating the silicon oxide and monocrystalline regions in an atmosphere with an arsenic compound, the layer of arsenic not being formed on the region of silicon oxide; and, thereafter,

2) forming a layer of non-monocrystalline silicon as an auxiliary layer on the region of silicon oxide by heating the semiconductor body in an atmosphere that includes a gaseous silicon compound and that does not include a gaseous arsenic compound, the layer of non-monocrystalline silicon not being formed on the region of monocrystalline silicon;

wherein the layer of arsenic is removed and then a silicon-containing layer is deposited on the region of monocrystalline silicon.

2. (Previously presented) A method as claimed in claim 1, wherein the semiconductor body is heated during Step 1) in an atmosphere comprising, in addition to the gaseous arsenic compound, the gaseous silicon compound used during Step 2).

3. (Previously presented) A method a claimed in claim 1, wherein Step 2) is ended before deposition from the silicon compound takes place on the arsenic layer formed on the region of monocrystalline silicon.

4. (Previously presented) A method as claimed in claim 1, wherein during the forming of the auxiliary layer, the semiconductor body is heated at a temperature in the range between 400 and 600°C in an atmosphere with a pressure below 500 mTorr.

5. (Currently Amended) A method as claimed in claim 1, further comprising, after the formation of the auxiliary layer, depositing ~~a~~ <u>the</u> silicon-containing layer on the arsenic layer and on the auxiliary layer by heating the semiconductor body in an atmosphere that includes a gaseous silicon compound, thereby forming a monocrystalline layer on the region of monocrystalline silicon and forming a polycrystalline layer on the auxiliary layer.

6. (Previously presented) A method as claimed in claim 5, wherein the silicon-containing layer is a layer of $Si_{1-x}Ge_x$, where $0.05<x<0.20$, and to which less than 0.2 at. % carbon is added, and wherein the semiconductor body is heated in an atmosphere comprising a silicon compound and a germanium compound.

7. (Previously presented) A method as claimed in claim 5, further comprising forming an n-type collector zone of a bipolar transistor in the region of monocrystalline silicon, and forming a p-type base zone of the bipolar transistor in the first monocrystalline layer.

8. (Previously presented) A method as claimed in claim 5, further comprising depositing a silicon layer on the arsenic layer and on the monocrystalline layer and on the polycrystalline layer by heating the semiconductor body in an atmosphere that includes a gaseous silicon compound, thereby forming a monocrystalline layer of silicon on the monocrystalline layer and forming a polycrystalline layer of silicon on the polycrystalline layer.

9. (Previously presented) A method as claimed in claim 8, further comprising depositing a silicon oxide layer on the monocrystalline layer of silicon and on the polycrystalline layer of silicon, etching the silicon oxide layer to form a window that exposes part of the monocrystalline layer of silicon, and providing an n-type doped polycrystalline silicon conductor track that contacts the monocrystalline layer of silicon through the window.

10. (Cancelled) ~~A method as claimed in claim 5, further comprising removing the layer of arsenic prior to depositing the silicon-containing layer, wherein the silicon-containing layer is deposited on the region of monocrystalline silicon.~~

11. (Currently Amended) A method ~~as claimed in claim 1~~ of manufacturing a semiconductor device on a region of silicon oxide situated next to a region of monocrystalline silicon at a surface of a semiconductor body, the method comprising:

1) forming a layer of arsenic on the region of monocrystalline silicon by heating the silicon oxide and monocrystalline regions in an atmosphere with an arsenic compound, the layer of arsenic not being formed on the region of silicon oxide; and, thereafter,

2) forming a layer of non-monocrystalline silicon as an auxiliary layer on the region of silicon oxide by heating the semiconductor body in an atmosphere that includes a gaseous silicon compound and that does not include a gaseous arsenic compound, the layer of non-monocrystalline silicon not being formed on the region of monocrystalline silicon, wherein the semiconductor body further includes a buried layer and a contact zone that is situated next to the region of silicon oxide at the surface of the semiconductor body, the contact zone extending from the surface of the semiconductor body to the buried layer, and wherein the layer of arsenic is also formed on the contact zone during step 1) and the layer of non-monocrystalline silicon is not formed on the contact zone during step 2).